What is claimed is:

1. A signal processing semiconductor integrated circuit comprising:

a reception circuit including a fist amplifier that amplifies a reception signal, a frequency conversion means that synthesizes an amplified signal and an oscillation signal of a specific frequency to form a frequency converted signal, and a second amplifier direct-current-coupled with the frequency conversion means, which amplifies the frequency converted signal by the frequency conversion means; and

a third amplifier that is activated while the first amplifier is deactivated, whose input terminal is not connected to an external terminal to which the reception signal is inputted.

2. A signal processing semiconductor integrated circuit according to Claim 1, wherein the input terminal of the third amplifier has an impedance connected which is equivalent to that of an external circuit connected to the input terminal of the first amplifier.

3. A signal processing semiconductor integrated circuit comprising:

a reception circuit including a fist amplifier that amplifies a reception signal, a frequency conversion means that

synthesizes an amplified signal and an oscillation signal of a specific frequency to form a frequency converted signal, and a second amplifier direct-current-coupled with the frequency conversion means, which amplifies the frequency converted signal by the frequency conversion means, and having a first operation mode in which the reception circuit is activated, and a second operation mode in which the reception circuit is deactivated; and

a third amplifier of which input terminal is not connected to an external terminal to which the reception signal is inputted,

wherein the second amplifier is provided with a calibration circuit that calibrates a direct current offset of the second amplifier, and

wherein the first amplifier is deactivated and the third amplifier is activated in response to shifting from the second operation mode into the first operation mode, and the calibration circuit calibrates the direct current offset of the second amplifier.

4. A signal processing semiconductor integrated circuit according to Claim 3, wherein the input terminal of the third amplifier has an impedance connected which is equivalent to that of an external circuit connected to the input terminal of the first amplifier.

5. A signal processing semiconductor integrated circuit according to Claim 3, wherein the third amplifier is deactivated and the first amplifier is activated, after the direct current offset is calibrated.

6. A signal processing semiconductor integrated circuit according to Claim 5, wherein the second amplifier has plural amplifier stages, and the amplifier stages each are provided with the calibration circuits that calibrate the direct current offsets.

7. A signal processing semiconductor integrated circuit formed on one semiconductor substrate, comprising:

the reception circuit according to Claim 3;

a transmission circuit that includes a modulation circuit that modulates a transmission signal, and an up-converting frequency conversion means that synthesizes a modulated signal and an oscillation signal to convert them into a higher frequency signal;

a control circuit that controls the reception circuit and the transmission circuit; and

an oscillation circuit that generates the oscillation signal synthesized by the reception circuit and the transmission circuit, or an oscillation control signal.

8. A wireless communication system comprising:

the signal processing semiconductor integrated circuit according to Claim 7; and

a base band circuit formed on a semiconductor substrate, which implements a signal processing, namely a conversion from a reception base band signal into an audio signal and a conversion from the audio signal into the base band signal, and a control of the signal processing semiconductor integrated circuit,

wherein the base band circuit supplies the signal processing semiconductor integrated circuit with a command signal to activate a reference voltage generation circuit that generates a bias voltage to a current source for supplying operation currents to the frequency conversion means and the second amplifier, and a command signal to activate the frequency conversion means and the second amplifier.

9. A wireless communication system according to Claim 8, wherein the command signal to activate the reference voltage generation circuit and the command signal to activate the frequency conversion means and the second amplifier are supplied from the base band circuit to the control circuit inside the signal processing semiconductor integrated circuit.

10. A control method in a signal processing semiconductor integrated circuit: comprising a reception circuit including a fist amplifier that amplifies a reception signal, a frequency conversion means that synthesizes an amplified signal and an oscillation signal of a specific frequency to form a frequency converted signal, and a second amplifier direct current-coupled with the frequency conversion means, which amplifies the frequency converted signal by the frequency conversion means, and a third amplifier of which input terminal is not connected to an external terminal to which the reception signal is inputted; and having a first operation mode in which the reception circuit is activated, and a second operation mode in which the reception circuit is deactivated,

wherein the direct current offset of the second amplifier is calibrated in a state that the first amplifier is deactivated and the third amplifier is activated in shifting from the second operation mode into the first operation mode.